TECHNICAL SPECIFICATIONS

HARDWARE

Digital Signal Processors

- One TI TMS320VC5409 DSP
- 100 MIPS per DSP processor
- On-chip memory: 32K word of SRAM, 16K word of ROM
- Local SRAM 128K x 16 for each DSP

Control Processor

- 32-bit ARM7 TDMI core
- 8K byte unified cache
- 4Kworde Write buffer
- Embedded on-chip Ethernet MAC with associated BDMA
- Local 2M x 16 SDRAM and 1M x 16 Flash

I/O

- Standard 10/100 BaseTX RJ 45 interface
- RJ 11 Loop Start interfaces for FXS/FXO

Mechanical, Environment & Power

- Dimension: L * W * H = 240.60 * 134.40 * 45.00 mm
- Operating temperature: 32 to 122 F (0℃ to 50℃)
- Operating humidity: 10% to 95% (non-condensing)
- Storage temperature: 14 to 140 F (-10 to 60℃)
- AC-to-DC power supply (90-260 VAC, auto-ranging, 50-60 Hz.)

Compliant

- CE
- FCC part 15 A
- FXS/FXO (Compliant with ITU-T G.712)
- UL

SOFTWARE

Speech

- Compression algorithms: ITU G. 711, G.723.1, and G.729A/B.
- Hybrid echo cancellation G.168 (16 ms)
- Auto switch between Fax and voice
- DTMF tone detection/regeneration
- Channel: four channels per module
- Comfort Noise Generation (CNG)
- User programmable Call Progress detection/generation
- Voice Activity Detection (VAD)
- User programmable Gain Control

Fax

- Facsimile protocol: T.30 Group 3
- Modulation formats: V.21, V.27*ter*, V.29, V.17
- Real-time fax over IP
- DTMF tone detection/regeneration

Management Tools

- RS 232 console port interface
- HTTP Server
- Telnet Server
- Elite Server for RAS and dial plan management
- TFTP and flash memory for remote software download and upgrade

H.323 Protocol Stack

- RAS sub-stack for Terminals and Gatekeepers: supports all mandatory and optional messages (Tx and Rx) as specified in table 19/H.255.0
- H.245 sub-stack: supports the Signaling Entities of Master Slave Determination, Capability Exchange, Open Logical Channels, and Close Logical Channels
- Q.931: supports all mandatory messages as specified in table 4/H.255.0
- Compliant with H.323 Version 1 and Version 2